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DVI-to-RGB (Sink) 2.0 IP Core User Guide

Revised October 9, 2019; Author Elod Gyorgy

1 Introduction

This user guide describes the Digilent DVI-to-RGB Video Decoder Intellectual Property. This IP interfaces directly to raw transition-minimized differential signaling (TMDS) clock and data channel inputs as defined in DVI 1.0 specs for Sink devices. It decodes the video stream and outputs 24-bit RGB video data along with the pixel clock and synchronization signals recovered from the TMDS link.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx®: IIC, vid_io Digilent: TMDS
Provided with core	
Design files	VHDL
Simulation model	VHDL Behavioral
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2018.2
Synthesis	Vivado Synthesis 2018.2

2 Features

- Connects directly to top-level digital visual interface (DVI) port
- 24-bit video (clocked parallel video data with synchronization signals) output
- Display Data Channel interface with built-in EDID ROM
- Resolutions supported: 1920x1080/60Hz down to 800x600/60Hz (148.5 MHz – 40 MHz)
- Selectable preferred resolution in EDID
- Xilinx interfaces used: IIC, vid_io
- Digilent interfaces used: TMDS

3 Performance

The IP constrains TMDS_Clk to 165 MHz, the maximum frequency outlined in DVI 1.0 specifications. However, depending on the actual FPGA part or speed grade, the maximum supported frequency might be lower. If the top-level design fails timing on pulse-width checks inside the IP instance, TMDS_Clk needs to be (re)constrained to the maximum frequency supported on the project part. Check the part datasheet for F_{MAX_BUFIO}, which is the most likely reason for failed timing. TMDS_Clk should be constrained for $F_{MAX\_BUFIO}/5$. Consequently, this is the maximum pixel clock frequency supported on that FPGA family and speed grade.

4 Overview

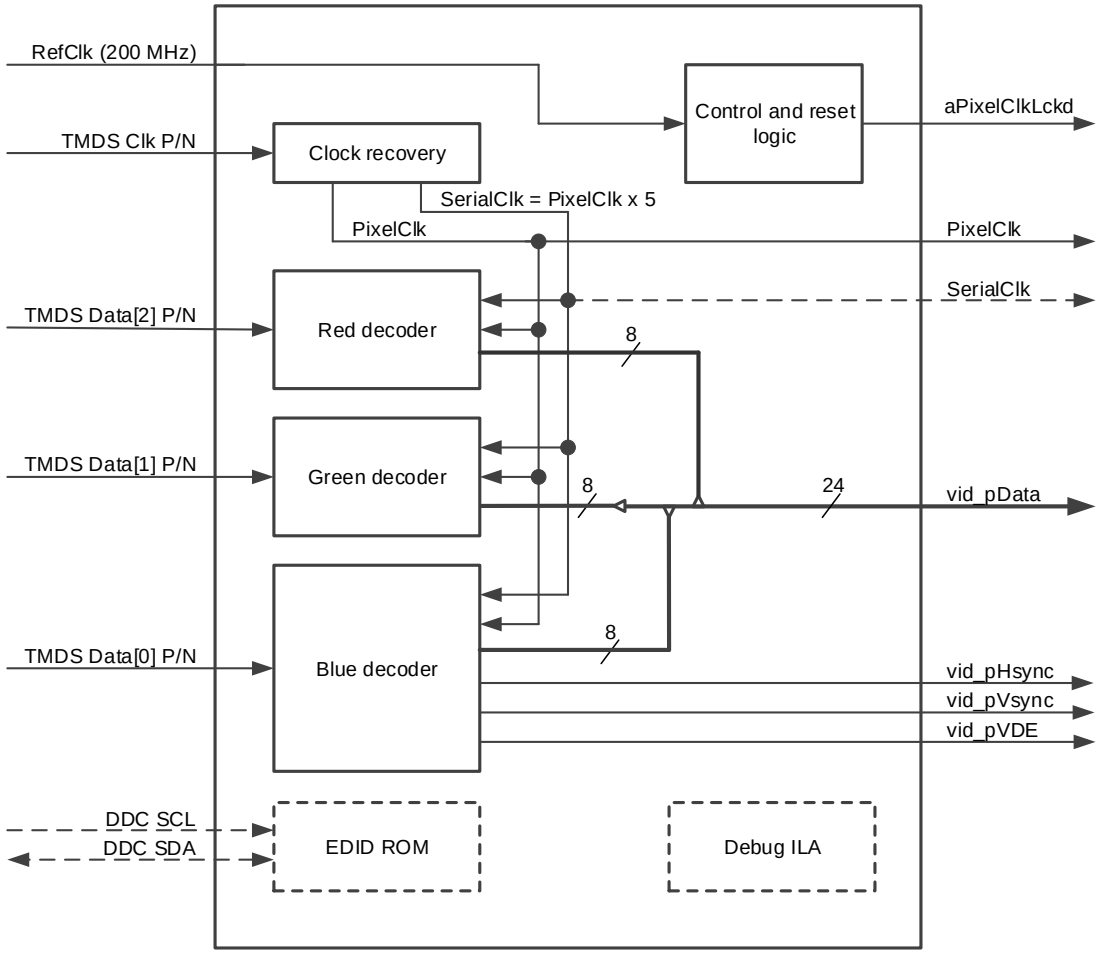

Figure 1. DVI to VGA converter block diagram.

The IP is built from multiple blocks: one clock recovery block, one data decoder block for each data channel (see [3], [4]), one optional DDC (Display Data Channel) block and one control/reset block.

4.1 Clock recovery

The clock channel carries a character-rate frequency reference. One character (or 10 bits) are transmitted every period on each data channel. Dedicated deserializer primitives, which require a fast serial clock, will be used to sample the serial data stream. The clock recovery block generates a serial clock and a pixel clock from the clock channel. The frequency ratio between the two clocks is 5:1.

Since the clock frequencies are relatively high and the recovered clocks have tight phase requirements, dedicated clocking primitives are instantiated inside this block. These can be seen in Figure 2. The MMCM primitive incorporates a voltage controlled oscillator (VCO) that has an operating range specified in the FPGA data sheet. Since there is no single set of MMCM parameters that maps the whole range of

DVI pixel clock frequencies to the VCO range, an IP customization parameter is available to optimize for the expected resolution and pixel clock frequency.

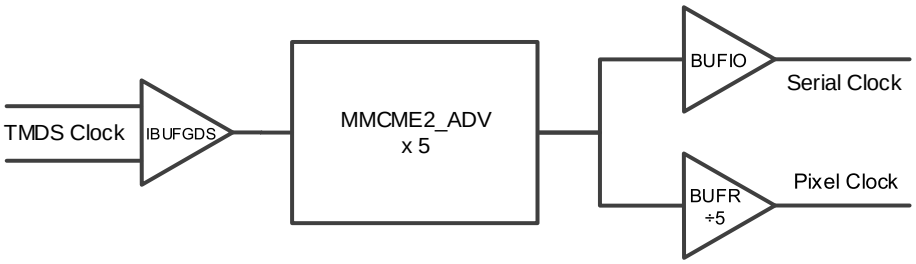

Figure 2. Clock network overview.

4.2 Data Decoder

There is no phase relationship between the recovered pixel clock or serial clock and the data channels. Furthermore, the data channels themselves are allowed a considerable skew between them. So the decoder block needs to align the phase of the serial clock with the data bit and find the character boundary in each data stream. Since this has to be done independently on each of the three data channels, it makes sense to vary the phase of the data streams while keeping the clock phase fixed.

4.2.1 Synchronization

To help with synchronization, the DVI protocol specifies period cues (control tokens) to be sent. These control tokens are sufficiently different from the rest of the data that their succession can be used for synchronization. Synchronization is automatically (re)started when a stable clock is detected and recovered. The time it takes for a lock to be achieved depends on the phase relationship of the clock and data streams. It should not last more than 1 minute.

DVI characters are 10-bits long, so a 10:1 deserialization of the data stream is needed. This can be achieved with two ISERDESE2 primitives in a cascaded DDR configuration. In this configuration, the master and slave ISERDESE2 take the serial data stream and sample it on both edges of a serial clock. Thus, for every five serial clock periods, ten data bits are sampled. This 10-bit data is then output synchronously with a divided clock, which is our pixel clock from the clock recovery block. Although this recovers 10-bit words from the data stream at a frequency which can be passed on to general logic inside the FPGA, it does guarantee the word actually starts at a character boundary or if the data stream is sampled when data is stable.

To find the best moment to sample the data stream (i.e., the middle of an open eye), an IDELAYE2 primitive is inserted in front of ISERDESE2. This primitive is capable of delaying the data signal in tap increments. In this IP, a 78ps increment is used for a total of 32 increments. For the highest pixel clock frequency supported (165 MHz), one bit period is covered in 7 tap increments. The goal is to find the tap delay value that shifts the data enough so that it gets sampled in the middle of its stable zone. The phase alignment module compares the 10-bit words with the four special control tokens. If a succession

of tokens is not recognized in a timeout period, we are in the jitter zone and it increments the tap delay. This is done repeatedly until control tokens are reliably recognized and the algorithm settles on the middle of the stable bit period (open eye). An “open eye” is defined by a succession of a minimum number of tap values (3) where the control token can be reliably detected, and it is delimited on both ends by a tap value where it cannot be. However, using this definition will miss open eyes that begin or end at the extremities of the tap delay range (0 or 31), because no two jitter zone delimiters will be found. So even if the open eye begins or ends in the extremities, if it is sufficiently long (16 tap increments), it will be considered a valid eye.

However, the IDELAYE2 primitive only provides a fine phase adjustment on the bit level, not covering the whole character. To find the character boundary, a coarse phase adjustment is needed. This is achieved by the “bitslip” feature of the ISERDESE2 primitive. If all the tap increments have been tried and control tokens are still not detected, it is assumed that we are not at the right character boundary. In this case, invoking “bitslip” causes either a shift right by one while bit or a shift left by three in the 10-bit word. After “bitslip” completes, phase alignment begins again, looping through the tap increments until tokens are found.

Phase alignment is considered completed when a succession of control tokens are reliably detected on all data channels. At this moment all three data channel are considered valid.

However, since inter-pair channel skew is not negligible and channels are aligned independently, the recovered data streams might have different delays on them. To eliminate this skew, the channels are bonded by buffering them in FIFO memories and holding them back independently until the video blanking period starts at the same time on all three. At this stage, all three data channels are valid and in-sync.

4.2.2 Decoding

The TMDS standard encodes data so that the serial data stream contains few transitions (0-to-1 or 1-to-0) and a DC balance (the same number of zeros and ones over a long time period). Every 10-bit character actually encapsulates 8 bits of useful data. The exception to this are the control tokens, which encapsulate 2 bits of control data. The data decoder block applies the decoding algorithm as specified in the DVI 1.0 specifications. After decoding we are left with control data in blanking periods or pixel data in active periods. Since each data channel carries one color, a 24-bit RGB pixel bus is output from the IP.

4.3 EDID ROM (Display Data Channel)

The DDC block emulates a read-only memory containing a default Digilent-branded extended display identification data (EDID). There are four variants available differing only in the preferred resolution. This parameter is user-selectable in the IP customization wizard. The EDID is defined in the src/*.data files bundled with the IP (see section 6.4). Upon synthesis, the file corresponding to the preferred resolution gets incorporated into the netlist. Modifying these files is allowed, provided it remains compatible with DDC specs.

5 Port Descriptions

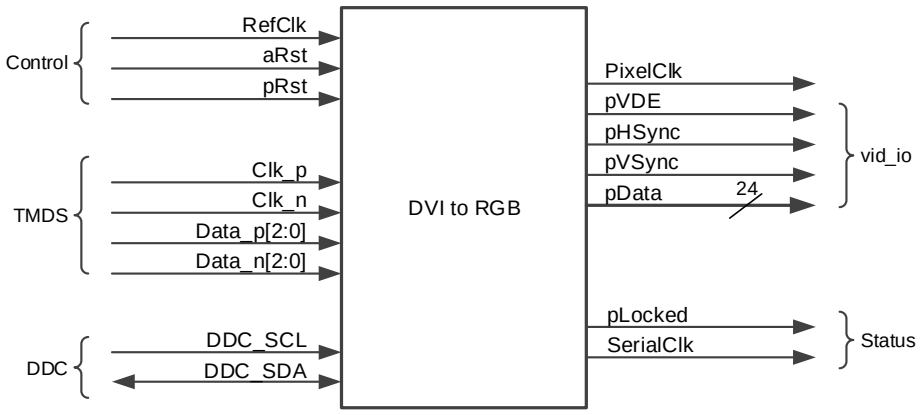

Figure 3. IP top-level diagram.

The signals of the DVI to VGA Core are listed and described in Table 1.

Signal Name	Interface	Signal Type	Init State	Description
RefClk	-	I	N/A	200 MHz reference clock.
aRst(_n)	-	I	N/A	Asynchronous reset of configurable polarity. Assert, if RefClk is not within spec.
pRst(_n)	-	I	N/A	Active-high reset synchronous with PixelClk. Configurable polarity.
Clk_p/Clk_n	tmds	I	N/A	DVI Clock Channel.
Data_p[2:0]/Data_n[2:0]	tmds	I	N/A	DVI Data Channel 0.
SCL	iic	I	N/A	Display Data Channel clock signal. Optional.
SDA	iic	IO	HiZ	Display Data Channel data signal. Optional.
PixelClk	rgb	O	N/A	Pixel clock recovered from the TMDS clock channel. Driven by BUFR.
pVDE	rgb	O	0	Video data valid: • 1 = Active video. • 0 = Blanking period.
pHSync	rgb	O	0	Horizontal synchronization video timing signal.
pVSync	rgb	O	0	Vertical synchronization video timing signal.
pData (23:0)	rgb	O	zeros	Video pixel data packed as RBG.

Signal Name	Interface	Signal Type	Init State	Description
pLocked	-	O	0	Active-high signal for locked status of PixelClk and SerialClk. De-asserted asynchronously, asserted synchronously to PixelClk. When zero, PixelClk is lost or not within specs.
SerialClk	-	O	N/A	Fast clock, toggling at five times the frequency of PixelClk. It is used internally for deserialization. Provided optionally as output for advanced use, like clocking an RGB2DVI core. Driven by BUFIO.

Table 1. Port descriptions.

6 Designing with the core

6.1 Constraints

The TMDS clock input Clk_p/n is constrained in the IP to the maximum DVI clock frequency, 165 MHz. On some architectures this might result in timing impossible to meet. Depending on the application, if a lower pixel clock frequency is acceptable, the clock can be constrained on top-level, which will override the IP-internal constraints.

For example, to constrain the design for 720p resolution (74.25 MHz), calculate de clock period (13.468 ns), and add the following to a project XDC file to constrain the clock on the top-level input port:

```
create_clock -period 13.468 -waveform {0.000 5.000} [get_ports
hdmi_rx_clk_p]
```

6.2 Customization

The IP provides the following customizable parameters: the polarity of reset signals, PixelClk clock buffer type, the frequency range of TMDS clock, the instantiation of debug logic, the preferred resolution to be declared in the bundled EDID, the availability of the DDC channel, and the serial clock output.

Enabling the DDC channel and serial clock will add the respective ports to the IP and are available to user logic.

The parallel pixel clock (PixelClk) is recovered by the use of a BUFR buffer. Since BUFR is restricted to a single clock region and the video data output from the core is synchronous to PixelClk, any downstream logic consuming video data is also restricted to this clock region. The option to re-buffer PixelClk introduces a BUFG after the BUFR and re-registers video data into the BUFG-domain. This will allow downstream logic to be placed anywhere on the device.

Setting the expected TMDS clock frequency enables the IP to instantiate FPGA primitives that respect timing requirements in the clock recovery logic. If the actual pixel clock recovered from the stream falls outside the range set here, the VCO operating range of the FPGA might not be respected and in extreme cases clock recovery might fail and the video stream will not be decoded properly.

The preferred resolution can be set, if the DDC channel is enabled. The resolution set here will select the proper initialization file for the emulated EDID ROM. This EDID will be read out by connected sources and *might* choose to transmit at this resolution.

Debug modules can be instantiated by enabling the option in the wizard. Enabling it result in two ILA cores being synthesized which can be used in Vivado Hardware Manager to analyze some internal status signals aiding debug.

6.3 Using SerialClk

While the fast serial clock is normally only used internally for deserialization, it is available and useful in other limited circumstances. The limitations arise from the fact that this clock has a frequency usually too large (five-times the PixelClk frequency) to clock user logic. For example, 1080p will result in a 742.5 MHz SerialClk. A BUFIO primitive drives this clock net to accommodate the large frequencies, which can only clock the I/O column in the same bank/clock region.

One case would be to use this clock to drive the Digilent RGB2DVI core, sharing the clocking logic between the two cores.

6.4 Bundled EDID

The IP comes with several EDID files each declaring a different preferred/native resolution.
Files named *.data contain 256 bytes of EDID data in a format readable by Vivado synthesis. Each line has exactly one byte in binary format. Byte 0 is the first in the file. The following table summarizes the EDID in a human-readable format. You may also find *.dat files in the docs/ directory that you may open in EDID editor tools.

Monitor	
Model name	Digilent DVI
Manufacturer	DGL
Plug and Play ID	DGL 720P CEA
Serial number	n/a
Manufacture date	2017, ISO week 36
Filter driver	None
EDID revision	1.3
Input signal type	Digital
Color bit depth	8 bits per primary color
Color encoding formats	RGB 4:4:4
Screen size	510 x 290 mm (23.1 in)
Power management	Not supported
Extension blocs	CEA Extension
DDC/CI	n/a

Color characteristics	
Default color space	Non-sRGB
Display gamma	2.20
Red chromaticity	Rx 0.6380 - Ry 0.3302
Green chromaticity	Gx 0.3117 - Gy 0.6233
Blue chromaticity	Bx 0.1505 - By 0.0684
White point (default)	Wx 0.3136 - Wy 0.3293
Additional descriptors	None

Timing characteristics	
GTF standard	Not supported
Additional descriptors	None
Preferred timing	Yes
Detailed timing	1280 x 720 at 60Hz 1920 x 1080 at 60Hz
Established timings	640 x 480p at 60Hz - IBM VGA 800 x 600p at 60Hz - VESA 1024 x 768p at 60Hz - VESA 1280 x 1024p at 60Hz - VESA STD

Table 2. Default EDID.

7 Debugging

Two ILA cores are added, when debug module is enabled, one for each clock domain: RefClk and PixelClk. The RefClk domain contains control logic that is alive even when no clock is being received on the TMDS interface. Signals related to reset and clock recovery are tied to this ILA.

Signal Name	Init State	Description
rDlyRst	1	Active-high reset signal for IDELAYCTRL primitive.
rRdyRst	1	Active-high reset signal for control logic that is asserted until IDELAYCTRL becomes ready.
rMMCM_Reset	1	Active-high reset for MMCM primitive doing clock recovery.
rBUFR_Rst	0	Active-high reset for BUFR primitive doing clock recovery. Pulses for one period, when MMCM achieves lock and the recovered clock is stable.
rMMCM_Locked	0	MMCM lock signal synchronized with RefClk.

Signal Name	Init State	Description
Clocking_Locked	0	The delayed version of the MMCM lock that takes into account the BUFR reset period to signal that all clock signals are now stable.

Table 3 Debug signals available in the RefClk domain ILA

The PixelClk domain ILA probes signals related to data decoding logic. The PixelClk ILA can be triggered from the RefClk ILA trig_out port too.

Signal Name	Init State	Description
pLockLostRst	1	Active-high reset signal for data decoding logic, when there is no stable PixelClk (Clocking_Locked is de-asserted).
pAlignErr[2:0]	0	Per-channel alignment error status signal. Alignment error happens when no valid tokens were found and all fine (intra-bit) alignment options are exhausted. Will trigger coarse (inter-bit) alignment attempt. Expected to happen during normal alignment attempts.
pBitslip[2:0]	0	Per-channel coarse alignment. Triggers the bitslip functionality of the ISERDESE2 primitives. Alignment should be achieved in at most 10 bitslip attempts.
pEyeSize[2:0][4:0]	0	Per-channel tap delay value in use after alignment lock. This value shows how many tap increments were showing valid data during fine alignment. The bigger the value, the better the signal quality.
pVld[2:0]	0	Per-channel status signal of data alignment. Asserted when intra-channel alignment is complete and the channel receives valid tokens. When all channels are valid, channel bonding starts
pRdy[2:0]	0	Per-channel status signal of channel bonding. Asserted when inter-channel alignment is achieved and channel skew is eliminated.

Table 4 Debug signals available in the PixelClk domain ILA

8 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *UG471: 7 Series FPGAs SelectIO Resources*, v1.3, October 31, 2012.
2. Xilinx Inc., *UG472: 7 Series FPGAs Clocking Resources*, v1.6, October 2, 2012.
3. Xilinx Inc., *XAPP460: Video Connectivity Using TMDS I/O in Spartan-3A FPGAs*, V1.1, June 24, 2011.

4. Xilinx Inc., *XAPP495: Implementing a TMDS Video Interface in the Spartan-6 FPGA*, v1.0, December 13, 2010.
5. Xilinx Inc., *WP249: SPI-4.2 Dynamic Phase Alignment*, v1.3, July 6, 2011.
6. DDWG: *Digital Visual Interface DVI*, Revision 1.0, April 2, 1999.